Laid-Open Application

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[Title of the Invention] Thin-Film Semiconductor Device

[Abstract]

[Subject] Re-crystallization process by laser annealing of a semiconductor thin film which is used as an active layer of a bottom-gate-type thin-film transistor, is unified and optimized.

[Solving Means] The thin-film semiconductor device refers to a device such that having thin film transistors 3 formed on an insulating substrate 1 in an integrated manner. The thin-film transistor 3 has a bottom-gate structure in which a gate electrode 5, an insulating film 4 and a semiconductor thin film 2 are stacked from the bottom in this order. The gate electrode 5 has a multi-layered structure comprising an upper layer 5a having a relatively low thermal conductivity and an electric conductivity sufficient for establishing contact, and a lower layer 5b having a relatively high thermal conductivity and an electric conductivity necessary for working as a wiring. The semiconductor thin film 2 is subjected to energy irradiation in a state extended over the gate electrode 5 and the insulating substrate 1 while placing the insulating film 4 thereunder, to thereby produce a polycrystalline structure r -crystallized in a uniform and optimized manner. In some cases, it is als all wable

t form a heat-conductive underlaid film so as to be placed in a plan view in adjacent to the gate electrode t thereby unify the heat conduction over the surface of the insulating substrate 1.

[Claims]

[Claim 1] In a thin-film semiconductor device having formed on an insulating substrate in an integrated manner thin-film transistors individually having a bottom-gate structure in which a gate electrode, an insulating film and a semiconductor thin film are stacked from the bottom in this order, said thin-film semiconductor device is characterized in that

said gate electrode has a multi-layered structure comprising at least an upper layer having a relatively low thermal conductivity and an electric conductivity sufficient for establishing contact, and a lower layer having a relatively high thermal conductivity and an electric conductivity necessary for working as a wiring, and

said semiconductor thin film has a polycrystalline structure re-crystallized by energy irradiation in a state extended over said gate electrode and said insulating substrate while placing said insulating film thereunder.

[Claim 2] The thin-film semiconductor device as claimed in Claim 1, characterized wherein

said gate electrode has a trapezoidal section.

[Claim 3] The thin-film semiconductor device as claimed in Claim 1, characterized in that

at least either of said upper layer and lower layer of said gate electrode has a light blocking effect.

[Claim 4] In a thin-film semiconductor device having formed on an insulating substrate in an integrated manner thin-film transistors individually having a bottom-gate structure in which a gate electrode, an insulating film and a semiconductor thin film are stacked from the

bottom in this order, said thin-film semiconductor device is characterized in that

said insulating substrate has formed on the surface thereof a heat-conductive underlaid film so as to be placed in a plan view in adjacent to said gate electrode to thereby unify the heat conduction over the surface of said insulating substrate, and

said semiconductor thin film has a polycrystalline structure re-crystallized by energy irradiation in a state extended over said gate electrode and said underlaid film while placing said insulating film thereunder.

[Claim 5] In a display device comprising a pair of insulating substrates bonded while keeping a predetermined gap in between, and an electro-optical material retained in said gap, on one insulating substrate having formed thereon an opposed electrode, and the other insulating substrate having formed thereon in an integrated manner thin-film transistors and pixel electrodes, said thin-film transistors individually having a bottom-gate structure in which a gate electrode, an insulating film and a semiconductor thin film are stacked from the bottom in this order, said display device is characterized in that

said gate electrode has a multi-layered structure comprising at least an upper layer having a relatively low thermal conductivity and an electric conductivity sufficient for establishing contact, and a lower layer having a relatively high thermal conductivity and an electric conductivity necessary for working as a wiring, and

said semiconductor thin film has a polycrystalline structure re-crystallized by energy irradiation in a state extended over said gate electrode and said insulating substrate while placing said insulating film thereunder.

[Claim 6] In a display device comprising a pair of insulating substrates bonded while keeping a predetermined gap in between, and

an electro-optical material retained in said gap, on one insulating substrate having formed thereon an oppos d electrode, and the other insulating substrate having formed thereon in an integrated manner thin-film transistors and pixel electrodes, said thin-film transistors individually having a bottom-gate structure in which a gate electrode, an insulating film and a semiconductor thin film are stacked from the bottom in this order, said display device is characterized in that

said other insulating substrate has formed on the surface thereof a heat-conductive underlaid film so as to be placed in a plan view in adjacent to said gate electrode to thereby unify the heat conduction over the surface of said other insulating substrate, and

said semiconductor thin film has a polycrystalline structure re-crystallized by energy irradiation in a state extended over said gate electrode and said underlaid film while placing said insulating film thereunder.

[Detailed Description of the Invention]

[0001]

[Field of the Invention] The present invention relates to a thin-film semiconductor device having formed on an insulating substrate in an integrated manner thin-film transistors individually having a bottom-gate structure in which a polycrystalline layer or the like is used as an active layer. The present invention more specifically relates to a structure of a polysilicon thin-film transistor manufactured by a low-temperature process below 600℃.

[0002]

[Description of Prior Art] Thin-film semiconductor device is suitable for use in a driving substrate for activ -matrix-type liquid crystal display or so in the field of display, and is under extensive developmental efforts at present. The active layer of the thin-film

transistor is composed of a polysilicon or amorphous silicon. In particular, polysilicon thin-film transistor attracts much attention with expectation of realizing an active-matrix-type color liquid crystal display having a small size and high definition. Since the display device contains thin-film transistors, working as pixel switching devices, formed on an insulating substrate such as a transparent glass, the device needs a new semiconductor technology for composing the active layer with a polysilicon thin film which has been used only as materials for electrodes and resistor. This is an only possible technology for producing thin-film transistors for high-performance switching capable of allowing high-density design, which is indispensable for achieving image quality which can satisfy the market's needs. This concomitantly enabled that the peripheral circuit portion, which has conventionally been provided as an externally-attached IC, can be formed on the same substrate in the same process with the pixel array portion. This successfully provides a high-definition, active-matrix-type liquid crystal display having an integrated peripheral circuit portion, which has never been realized by amorphous-silicon type thin-film transistors.

[0003] Since polysilicon is larger in carrier mobility than amorphous silicon, the polysilicon thin-film transistor can gain a higher current driving performance, which makes it possible to fabricate the peripheral circuit portion such as horizontal scanning circuit and vertical scanning circuit, both of which being in need of high-speed operation, on the same substrate at the same time with thin-film transistors for pixel switching. Thus the number of signal lines drawn out from a thin-film semiconductor display device can be reduced to a large extent. Another advantage resides in that a CMOS circuit having formed th rein an n-channel type thin-film transistor and a p-channel type thin-film transistor in an integrated manner can be pr vided as an on-chip circuit, which promotes a built-in

constitution of a level-shift circuit, and ensures low-voltage operation of timing-related signals.

[0004] Device technology and process technology for thin-film transistor have conventionally been established as high-temperature process technologies employing process temperatures of 1,000℃ or above. The high-temperature process is characterized in that modifying, through solid phase growth, a semiconductor thin film previously formed on a highly heat-resistant substrate such as a quartz substrate. The solid phase growth method refers to a process of annealing a semiconductor thin film at a temperature of 1,000℃ or above, where the film forming process of which is responsible for enlarging the individual crystal grains contained in polysilicon which is an aggregation of fine silicon crystals. Polysilicon obtained by the solid phase growth method has a carrier mobility of as large as 100 $cm^2/v \cdot s$ or around. It is, however, essential to use a substrate excellent in heat resistance for successfully carrying out the foregoing high-temperature process, thus the conventional practice was to use expensive quartz. But the quartz is disadvantageous from a viewpoint of saving the production cost.

[0005] In place of the foregoing high-temperature process, there is proposed a low-temperature process using a process temperature of 600℃ or below. As one strategy for lowering the process temperature in manufacturing processes of the thin-film semiconductor device, laser annealing using laser beam attracts much attention. According to the method, a laser beam is irradiated on an amorphous semiconductor thin film comprising amorphous silicon or polysilicon formed on an insulating substrate having a low heat resistance, to thereby locally heat and fuse the thin film, and then allows the semiconductor thin film to re-crystallize during the cooling process. Thus re-crystallized semiconductor thin film is used as the active layer (channel region) to thereby compose the

polysilicon thin-film transistors in an integrated manner. The re-crystallized semiconductor thin film has a larger carrier mobility than before, and can upgrade the performance of the thin-film transistor to a certain extent.

[0006] In the conventional field of thin-film transistors, those having a top-gate structure have been the mainstream. In the top-gate structure, a semiconductor thin film is formed on an insulating substrate, and a gate electrode is placed over it while placing a gate insulating film in between. A low-cost and large-sized glass plate is now available as the insulating substrate for the low-temperature process. The glass plate, however, contains a large amount of impurity metals such as Na which can localize depending on voltage for driving the thin-film semiconductor. This is undesirable from a viewpoint of reliability since the resultant electric field varies characteristics of the thin-film transistor. On the contrary, recent efforts have succeeded in developing a bottom-gate structure, in which a gate electrode comprising a metal film or so is placed on an insulating substrate made of a glass plate or the like, and a semiconductor thin film is formed over it while placing a gate insulating film in between. The gate electrode can shield an electric field in the glass plate, and by virtue of the structural feature, the bottom-gate-type transistor is superior to the top-gate-type one in terms of reliability. Fig. 7 shows comparative data of reliability of the bottom-gate-type and top-gate-type thin-film transistors for reference. The data was obtained by composing a CMOS ring oscillator using the thin-film transistors and by measuring time-dependent fluctuation in the oscillation frequency under a temperature condition of 120℃. As clearly known from Fig. 7, the bottom-gate-type product shows operation characteristic more stable than that of the top-gate-type one.

[0007]

[Problems t be Solved by the Invention] How ver, the bottom-gate-type structure has a seri us problem related to re-crystallization by laser annealing. The semiconductor thin film to be re-crystallized is provided so as to approximately locate the portion thereof where the channel region is to be formed just over the gate electrode, and so as to locate the portion thereof where the source and drain regions are to be formed over the glass plate. Provision of energy through laser beam irradiation will thus make difference in status of heat conduction and dissipation between the portions over the glass plate and over the metal gate electrode. This means that optimum laser energy will differ between the channel region and source/drain region, and that it becomes impossible to irradiate laser beam at an optimum energy which is beneficial for achieving a large carrier mobility. More specifically, the re-crystallization by laser annealing is carried out so as to irradiate laser beam on both of the semiconductor thin film over the metal gate electrode and that over the glass plate at the same time, where in the process of cooling for solidification after being once melted, the semiconductor thin film over the metal gate electrode can solidify relatively in a short time since the heat can conduct through the gate line and dissipate in the horizontal direction. This undesirably results in different sizes of the re-crystallized crystal grain in the portions of the semiconductor thin film over the metal gate electrode and over the glass plate, which makes the carrier mobility non-uniform. In an extreme case, an effort of obtaining larger grain size of the semiconductor thin film over the metal gate electrode can even result in vaporization of the semiconductor thin film over the glass plate due to an excessive energy of irradiation. Conversely, an effort of obtaining normal crystal state of the semiconductor thin film over the glass plate may result in only a small grain size of the semiconductor thin film over the metal gate electrode. This is a

problem to be solved in relation to the conventional bottom-gate structure.

[0008]

[Means for Solving the Problems] The following measures were taken in order to solve the above-described problems in the prior art. According to the present invention, a thin-film semiconductor device has, as a basic constitution, formed on an insulating substrate in an integrated manner thin-film transistors individually having a bottom-gate structure in which a gate electrode, an insulating film and a semiconductor thin film are stacked from the bottom in this order. A specific feature of the device relates to that the gate electrode has a multi-layered structure comprising at least an upper layer having a relatively low thermal conductivity and an electric conductivity sufficient for establishing contact, and a lower layer having a relatively high thermal conductivity and an electric conductivity necessary for working as a wiring. Another feature relates to that the semiconductor thin film has a polycrystalline structure re-crystallized by energy irradiation of the film in a state extended over the gate electrode and the insulating substrate while placing the insulating film thereunder. The gate electrode more-preferably has a trapezoidal section. At least either of the upper layer and lower layer of the gate electrode more preferably has a light blocking effect.

[0009] According to another aspect of the present invention, in a thin-film semiconductor device wherein thin-film transistors individually having a bottom-gate structure in which a gate electrode, an insulating film and a semiconductor thin film are stacked from the bottom in this order, are formed on an insulating substrate in an integrated manner, it is characterized that the insulating substrate has formed on the surface thereof a heat-conductive underlaid film so as to be placed in a plan view in adjacent to the gate electr de

t thereby unify the heat conduction over the surface of the insulating substrate. In this case, the semiconductor thin film has a polycrystalline structure re-crystallized by energy irradiation of the film in a state extended over the gate electrode and the underlaid film while placing the insulating film thereunder.

[0010] According to the first aspect of the present invention, the gate electrode is composed so as to have a stacked structure which contains the upper layer having a relatively low thermal conductivity and an electric conductivity sufficient for establishing contact. This successfully reduces difference in the heat conductivity between the portions over the gate electrode and over the insulating substrate, which makes it possible to optimize the laser energy and to produce high-quality polycrystalline semiconductor thin film. A problem herein arises that a material having a low thermal conductivity generally suffers from a low electric conductivity. This is disadvantageous for use in the gate wiring. The present invention thus suppresses the resistivity by providing the lower layer having an electric conductivity necessary for working as a wiring. As described above, to unify heat distribution over the entire surface of the insulating substrate, it is desirable to reduce thermal conductivity of a conductive material used for composing the gate electrode, whereas the resistivity as smaller as possible is desirable for the gate electrode. Since these two physical properties are contradictory in general, the first aspect of the present invention overcomes the problem by employing the double-layered structure for the gate electrode to thereby make best use of advantages of the upper and lower layers. According to the second aspect of the present invention, the heat-conductive underlaid film is formed so as to be placed in a plan view in adjacent to the gate electrode to thereby unify the heat conduction over the surface of the insulating substrate. This makes it possible to unif rmly re-crystallize the semiconductor

thin film by laser annealing, and to optimize conditions for irradiating the laser beam.

[0011]

[Embodiments of the Invention] Embodiments of the present invention will be detailed below referring to the attached drawings. Fig. 1 is a schematic partial sectional view of a first embodiment of the thin-film semiconductor device according to the present invention. As shown in the figure, the thin-film semiconductor device has formed on an insulating substrate 1 in an integrated manner thin-film transistors 3 individually having a bottom-gate structure in which a gate electrode 5, an insulating film 4 and a semiconductor thin film 2 are stacked from the bottom in this order. This type of thin-film semiconductor device is used for a driving substrate for an active-matrix-type display device. Accordingly, a pixel electrode 14 is connected to the thin-film semiconductor transistor 3. Further the thin-film transistor 3 has a double-gate structure in order to improve the reliability. It is, however, to be noted that the present invention is by no means limited thereto, and is of course also applicable to a thin-film transistor having a single-gate structure. When a display device is assembled, an insulating substrate 60 is bonded with the other insulating substrate 1 while keeping a predetermined gap in between. The insulating substrate 60 comprises a glass or the like, and has preliminarily formed on the surface thereof an opposed electrode 61. The gap between both substrates 60, 1 typically retains liquid crystal 50 as an electro-optical material.

[0012] A specific feature of the present invention resides in that the gate electrode 5 has a multi-layered structure in which at least an upper layer 5a and a lower layer 5b are stacked. The upper layer 5a has a relatively low thermal conductivity and an electric conductivity sufficient for establishing contact, and is typically composed of a compound film such as ITO film, TiN film or TiON film,

or of an alloy film such as nichrome film. Thickness of the film typically ranges from 50 nm to 300 nm or around. On the other hand, the lower layer 5b has a relatively high thermal conductivity and an electric conductivity necessary for working as a wiring, and is typically composed of a low-resistivity refractory metal film such as a film of W, Cr, Mo, Ti and so forth. Thickness of the film ranges from 50 nm to 200 nm, and is typically set at 100 nm. The gate electrode 5 is an extended portion of a gate line (not shown). The gate line generally has the same multi-layered structure with the gate electrode 5, and is connected to other circuit section (not shown) through a contact hole (not shown). For this reason, the upper layer 5a has an electric conductivity at least sufficient for establishing contact, and the lower layer 5b has an electric conductivity necessary for working as a wiring. The gate electrode 5 has a trapezoidal section. Angle of inclination of the side planes is 45° or less, and preferably falls within a range from 5° to 15°. The trapezoidal shape is advantageous in that preventing mis-coverage of film to be formed thereon. At least either of the upper layer 5a and lower layer 5b of the gate electrode 5 has a light blocking effect, so that the gate electrode 5 as a whole is opaque. This successfully suppresses current leakage from the thin-film transistor 3 induced by incident light coming from a back surface of the insulating substrate 1.

[0013] The gate electrode 5 is covered with the insulating film 4 typically made of SiO_2. On the insulating film 4, the semiconductor thin film 2 typically made of polysilicon is formed. Further on the semiconductor thin film 2, stoppers 6 are patterned so as to be aligned with the individual gate electrodes 5. Portions of the semiconductor thin film 2 which fall just under the stopper 6 will serve as channel regions. The semiconductor thin film 2 also has formed therein a source region 7 and a drain region 8 containing impurities implanted at high concentrations, and has further formed therein LDD regions

71, 78, 81 containing impurities implanted at low concentrations. Thus-composed thin-film transistor 3 is covered with an inter-layer insulating film 9 typically made of SiO_2. On the inter-layer insulating film 9, a signal line 10 is patterned and electrically connected to the source region 7 of the thin-film transistor 3 through a contact hole. The signal line 10 has a double-layered structure which comprises an upper metal film 10a typically made of Mo, and a lower metal film 10b typically made of Al. The line 10 for connection is patterned and connected also on the side of the drain region 8. These lines 10 are covered with a passivation film 11 and then with a planarization film 12. On the planarization film 12, a pixel electrode 14 typically made of ITO is patterned. The pixel electrode 14 is electrically connected to the drain region 8 of the thin-film transistor 3 through the contact hole and the line 10 for connection formed at the planarization film 12.

[0014] A method for manufacturing the thin-film semiconductor device shown in Fig. 1 will be detailed below referring to Fig. 2. It is to be noted that the drawing shows only one gate electrode for simplicity. First as shown in drawing (A), the lower layer 5b is formed typically by sputtering on the entire surface of the insulating substrate 1 typically made of glass. The lower layer 5b preferably has a low resistivity and further preferably has a high melting point, so that the layer is generally made of a metal film of W, Cr, Mo, Ti or the like. The thickness of the layer is approx. 100 nm, where a general allowable range thereof is 50 nm to 200 nm. On the entire surface of the lower layer 5b, the upper layer 5a is formed typically by sputtering in a continuous or discontinuous manner. The upper layer 5a presents a specific feature of the present invention. While the upper layer 5a needs not be so small in resistivity, a material having a small heat conductivity is used therefor. Even though being inappropriate as a wiring, it is still necessary for the upper layer

5a to have an electric conductivity sufficient for establishing contact. Thus the upper layer 5a is typically composed of a compound film such as ITO film, TiN film or TiON film, or of an alloy film such as nichrome film. Relatively large thickness thereof is preferable, and is generally set within a range from 50 nm to 300 nm or around.

[0015] Next as shown in drawing (B), the multi-layered film comprising a stack of the upper layer 5a and lower layer 5b is patterned typically by isotropic dry etching, to thereby obtain the gate electrode 5. The isotropic dry etching is successful in creating the trapezoidal section of the gate electrode 5. The gate electrode 5 is thus tapered so as to have the end planes thereof inclined at 5° to 15°.

[0016] Next as shown in drawing (C), an SiO_2 film is deposited typically by plasma-enhanced CVD (PE-CVD method) process typically in a thickness of 100 nm to 200 nm, to thereby form the insulating film 4 which covers the gate electrode 5. Further thereon amorphous silicon is deposited typically in a thickness of 20 nm to 60 nm to thereby form the semiconductor thin film 2. The insulating film 4 and semiconductor thin film 2 can successively be grown in the same film forming chamber without breaking the vacuum status. The insulating substrate 1 is then heated to 400℃ for example. The semiconductor thin film 2 formed by the PE-CVD process and composed of amorphous silicon contains hydrogen as much as 10% or around, and the hydrogen is released during the annealing at 400℃. Thereafter an XeCl excimer laser having a wavelength of 308 nm is then irradiated to the semiconductor thin film 2 for re-crystallization. The amorphous silicon is once melted by energy of the laser beam, and then solidifies to produce polysilicon. Length of time for the solidification governs the crystallinity (mainly grain size). A material having a relatively small heat conductivity is used for the upper layer 5a of the gate electrode 5 in the present invention, which

c rrespondently reduces the horizontal thermal diffusion and delays the solidification after the fusion. This desirably produces a polysilicon having a grain size large enough for the practical use. Another advantage resides in that the gate electrode 5 is processed so as to have the trapezoidal form, which successfully prevents mis-coverage of the semiconductor thin film 2 at step portions.

[0017] Next as shown in drawing (D), SiO_2 is deposited on the semiconductor thin film 2 by the PE-CVD process. The obtained SiO_2 film is then patterned using back-side exposure technique so as to obtain the stopper 6. The back-side exposure herein is effected in a self-aligned manner using the gate electrode 5 having a light blocking effect as a mask, so that the resultant stopper 6 is obtained as being aligned with the gate electrode 5. An impurity (phosphorus, for example) is then implanted at a relatively low concentration to the semiconductor thin film 2 by the ion doping process using the stopper 6 as a mask. The stopper 6 and the peripheral area are then covered with a photo-resist layer, and an impurity (phosphorus, for example) is again implanted at a relatively high concentration to the semiconductor thin film 2 by the ion doping process. The source region 7 and drain region 8 are thus formed, and portions in the semiconductor thin film 2 covered with the resist layer are remained as LDD regions 71, 81. The photo-resist layer which has become no more necessary is then removed. The ion doping process is a technique for doping ions in a plasma state into the semiconductor thin film 2 after being accelerated at a breath by the electric field.

[0018] Lastly as shown in drawing (E), the laser beam is irradiated again to activate the doped atoms. This is a technique same as that used for the re-crystallization, but requires only a small energy since there is no need to grow the crystal grain. An SiO_2 film is then deposited to form the inter-layer insulating film 9 for isolating the wirings. After contact holes are formed in the

inter-layer insulating film 9, metal aluminum or the like is deposited by sputtering, and the resultant film is then patterned in a predetermined shape to thereby fabricate the line 10. In the processes thereafter for manufacturing a thin-film semiconductor display device, a passivation film, planarization film and pixel electrode are formed as required.

[0019] Fig. 3 is a schematic expression of temperature change in the semiconductor thin film during the laser annealing. In a typical laser annealing, excimer laser light is irradiated in a pulse mode. Upon irradiation of the pulse, temperature of silicon (Si) composing the semiconductor thin film sharply rises and exceeds the melting point thereof. The steady state is thereafter kept for a while, and the temperature of Si gradually decreases upon completion of the pulse irradiation to reach the room temperature, during which silicon once melted solidifies to thereby produce a polycrystalline state. The cooling process depends on the thermal conductivity of the underlying gate electrode. As indicated by curve (1), a gate electrode comprising a conventional single-layered metal layer causes sharp drop of the temperature of silicon. In contrast as indicated by curve (3), silicon on an insulating substrate typically composed of a glass causes a relatively slow cooling, since glass is lower in thermal conductivity than metal or so. Curve (2) expresses a cooling curve obtained when the upper layer of the gate electrode is composed with a material which has a relatively low thermal conductivity according to the present invention. As is clear from the graph, the curve (2) approaches curve (3). In other words, the present invention is successful in reducing difference in the duration of time from melting to solidification of silicon between the portions over the glass and over the gate electrode. This makes it possible to obtain silicon having almost uniform crystal status irrespective of the underlying materials, and t optimize conditions for laser annealing.

[0020] Fig. 4 shows another embodiment of a method for forming the gate electrode 5. As shown in drawing (A), a metal film for forming the lower layer 5b is deposited on the insulating substrate 1 made of such as glass by sputtering. The metal film is typically formed with Ti in a thickness of 200 nm. Next as shown in drawing (B), the lower layer 5b is patterned into a form of the gate electrode. Further as shown in drawing (C), the surface of the lower layer 5b is modified to produce the upper layer 5a. More specifically, annealing of the lower layer 5b in a nitrogen atmosphere can produce the upper layer 5a composed of TiN. Thus the gate electrode 5 having a multi-layered structure which comprises the upper layer 5a and lower layer 5b is obtained. The residual processes thereafter are similar to those shown in Fig. 2.

[0021] Fig. 5 is a schematic partial sectional view of a second embodiment of the thin-film semiconductor device according to the present invention. For easy understanding, portions corresponded to those in the first embodiment previously shown in Fig. 1 are indicated by the same reference numerals. Again in the present embodiment, thin-film transistors 3 individually having a bottom-gate structure in which a gate electrode 5, an insulating film 4 and a semiconductor thin film 2 are stacked from the bottom in this order, are formed on the insulating substrate 1 in an integrated manner. A specific feature of the present embodiment relates to that a heat-conductive underlaid film 20 is formed on the surface of the insulating substrate 1 composed of glass or the like so as to be placed in a plan view in adjacent to the gate electrode 5 to thereby unify the heat conduction over the surface of the insulating substrate 1. In this connection, the gate electrode 5 is composed as a single-layered metal film typically made of Cr, Mo or Ta. On the other hand, the und rlaid film 20 is composed of a transparent electro-conductive film such as ITO film. The semiconductor thin film 2 has a polycrystalline structure

re-crystallized by energy irradiation of the film in a state extended over the gate electrode 5 and the underlaid film 20 while placing the insulating film 4 thereunder. As described in the above, the bottom-gate-type, thin-film transistor of the present embodiment employs the underlaid layer 20 having a heat conductivity larger than that of glass around the gate electrode 5 so as to unify the heat distribution during re-crystallization of the semiconductor thin film 2 by laser annealing. Thus the polycrystalline structure can be obtained with a desirable quality.

[0022] Fig. 6 is a schematic perspective view of an exemplary active-matrix-type liquid crystal display device assembled using, as a driving substrate, the thin-film semiconductor device of the present invention. The display device is composed so that an electro-optical material 50 typically comprising a liquid crystal is retained in a gap between the driving substrate 1 and an opposed substrate 60. The driving substrate 1 has formed thereon a pixel array portion and a peripheral circuit portion in an integrated manner. The peripheral circuit portion is divided into a vertical scanning circuit 41 and a horizontal scanning circuit 42. On the upper end side of the driving substrate 1, there is also provided terminal electrodes 47 for external connection. The individual terminal electrodes 47 are connected through wirings 48 with the vertical scanning circuit 41 and the horizontal scanning circuit 42. The pixel array portion has formed therein gate lines 43 and signal lines 10 crossing with each other. The gate lines 43 are connected to the vertical scanning circuit 41, and the signal lines 10 are connected to the horizontal scanning circuit 42. At each intersection of both lines 43, 10, the pixel electrode 14 and the thin-film transistor 3 for driving thereof are formed. On the other hand, the opposed substrate 60 has formed on the inner surface thereof opposed electrodes, although not shown.

[0023]

[Effect of the Invention] As has been described in the above, according to a first aspect of the present invention, the gate electrode has a multi-layered structure comprising an upper layer having a relatively low thermal conductivity and an electric conductivity sufficient for establishing contact, and a lower layer having a relatively high thermal conductivity and an electric conductivity necessary for working as a wiring. With this constitution, the semiconductor thin film is subjected to energy irradiation in a state extended over the gate electrode and the insulating substrate while placing the insulating film thereunder, which makes it possible to produce a polycrystalline structure re-crystallized in a uniform and optimized manner. According to a second aspect of the present invention, a heat-conductive underlaid film is formed on the surface of the insulating substrate so as to be placed in a plan view in adjacent to the gate electrode, which makes it possible to unify the heat conduction over the surface of the insulating substrate. The semiconductor thin film is subjected to energy irradiation in a state extended over the gate electrode and the under laid film while placing the insulating film thereunder, which makes it possible to produce a polycrystalline structure re-crystallized in a uniform and optimized manner.

[Brief Description of the Drawings]

[Fig. 1] It is a partial sectional view showing a first embodiment of the thin-film semiconductor device according to the present invention;

[Fig. 2] They are process drawings showing a method for manufacturing in relation to the first embodiment;

[Fig. 3] It is a graph for expressing temperature changes of semiconductor thin films during laser annealing;

[Fig. 4] They are process drawings showing another example of

a method for manufacturing the thin-film semiconductor device according to the present invention;

[Fig. 5] It is a partial sectional view showing a second embodiment of the thin-film semiconductor device according to the present invention;

[Fig. 6] It is a schematic perspective view showing an exemplary active-matrix display device assembled using the thin-film semiconductor device according to the present invention; and

[Fig. 7] It is a graph for comparatively explaining reliability of a bottom-gate-type thin-film transistor and a top-gate-type thin-film transistor.

[Explanation of the Marks]

1 ··· insulating substrate, 2 ··· semiconductor thin film, 4 ··· insulating film, 5 ··· gate electrode, 7 ··· source region, 8 ··· drain region, 9 ··· inter-layer insulating film, 10 ··· signal line, 14 ··· pixel electrode, 20 ··· underlaid layer

Fig. 1

1 insulating substrate

2 semiconductor thin film

3 thin-film transistor

4 insulating film

5 gate electrode

5a upper layer

5b lower layer

9 inter-layer insulating film

14 pixel electrode

Fig. 2 (A)

glass

Fig. 3

temperature

melting point of Si

time

laser pulse

time (nsec)

Fig. 4 (A)

glass

Fig. 5

1 insulating substrate

2 semiconductor thin film

3 thin-film transistor

4 insulating film

5 gate electrode

9 inter-layer insulating film

14 pixel electrode

20 underlaid film

Fig. 7

change rate of oscillation frequency (%)

time (H)

○ bottom-gate

□ top-gate